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RAINEY, ROBERT R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,605	STEER, WILLIAM A	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8* is/are allowed.

6)☒ Claim(s) *1-7 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/17/2008 with respect to the rejection of claims 1 and 10 under 35 U.S. C. §103 have been fully considered but are not persuasive.

Applicant argues the newly added limitation that "the linear operating region of the drive transistor is avoided" is not taught by Akimoto because Akimoto is silent about any operating, or not operating, transistors in any particular regions including avoiding the linear operating region. Examiner disagrees. The art and reading thereof already of record sufficiently describes the limitation added. The rejections below more clearly point out how the art applies to the new limitation and by way of further explanation examiner offers:

Akimoto describes a pulse-width-modulated gray scale. Pulse-width-modulation is an on-off type of modulation. It is known to be used specifically to avoid running transistors in their linear regions. One of ordinary skill in the art knows this without it being pointed out in so many words. Akimoto proposes in one embodiment, using a linear ramp input to a comparator in order to time the duration of the pulses. Akimoto recognizes that this could cause the circuit to pass through the linear region slowly and offers solutions to the problem. Akimoto provides elements so that the transition is made quickly through the transition point. Consider 6:1-8, especially "almost rectangular". Akimoto goes on to offer that further improvement can be obtained by using a stepped rather than linear waveform so that noise can be avoided (see Fig. 10 and citations in

rejections). Using a stepped waveform to drive a circuit designed to produce an "almost rectangular" response when driven by a linear voltage ramp makes the transition time even less. Clearly this avoids the linear region of operation of the transistors. Akimoto does not specifically state "my circuit avoids operating the drive transistor in the linear region" but the totality of the disclosure would have reasonably suggested it to one of ordinary skill in the art. Applicant is urged to describe, as limitations in the claims, the particular elements or methods that cause the linear region to be avoided, which applicant believes distinguish applicant's invention from the prior art.

Note

In the following rejections, primarily copied from the previous office action, the modifications for form and grammar have not been incorporated into the language of the rejections.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-7, 9-14 and 16-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,876,345 to *Akimoto et al.* ("*Akimoto*").

As to **claim 1**, *Akimoto* sixth embodiment discloses an active matrix electroluminescent display device comprising an array of display pixels (see for example column 5 lines 5-10 and column 1 lines 36-42), each pixel comprising: an electroluminescent display element (see for example Fig. 13 item 84 and column 12 line 35) and ; a drive transistor (see for example Fig. 13 item 91 and column 12 lines 30-36) for driving a current through the display element, a drive voltage being provided to the gate of the drive transistor (see for example Fig. 3 and column 5 lines 40-42, which generally teaches to Vin to Vout relationship); and a storage capacitor (see for example Fig. 13 item 82 and column 12 lines 25-30) for storing a drive level (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55) and connected between an input to the pixel and the gate of the drive transistor (see for example Fig. 13, which shows capacitor 82 so connected), wherein driver circuitry is provided for providing a linear voltage waveform to the input of the pixel (see for example Fig. 14 "PIXEL DRIVING VOLTAGE" associated with "DRIVING SIGNAL LINE" and column 12 lines 55-60), the voltage waveform being voltage-shifted by the storage capacitor before application to the gate of the drive transistor (see for example Fig. 13 and column 12 lines 51-60, which describe the storage of a signal voltage on the capacitor followed by the application of a triangular waveform to the capacitor through line 96; this results in the triangular waveform being voltage-shifted by the amount of the stored signal voltage before being applied to the gate of the drive transistor).

Akimoto sixth embodiment does not expressly disclose that the voltage waveform is stepped or that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor.

Akimoto third embodiment discloses that the voltage waveform is stepped and that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor so that the linear operating region of the drive transistor is avoided (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter and thus the drive transistor, i.e. item 31 or 32 of Fig. 6, is off at one step and on at another, and further that setting the writing signal at a medium level ensures that the switch point, i.e. linear operating region, is crossed in the transition from one step to another; since this is indicated as a stepped transition the linear operating region is "avoided", that is the transition through this region is rapid).

Akimoto sixth embodiment and *Akimoto* third embodiment are analogous art because they are from the same field of endeavor, which is image displays capable of multilevel display, and seek to solve the same problem, which is to reduce the variation in PWM circuits caused by differences between TFT circuitry.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the stepped waveform of *Akimoto* third embodiment to the circuit of *Akimoto* sixth embodiment. The

suggestion/motivation would have been to provide advantages such as to prevent changes caused by noise (see for example column 10 lines 11-14).

As to **claim 2**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third embodiment further discloses that the height of the steps in the stepped voltage waveform is sufficient to include the linear operating region voltages of the drive transistors of all pixels of the display (ibid. note that fig. 10 is representative of all pixels and thus applies to all drive transistors).

As to **claim 3**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third embodiment further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor (ibid. note that Fig. 10 shows two different stored levels and that each of these is set at a midpoint between step levels; further see for example 10:15-21).

As to **claim 4**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third embodiment further discloses that each pixel further comprises an address transistor, connected

between a power supply line and the gate of the drive transistor (see for example Fig. 13 item 89), and *Akimoto* third embodiment further discloses that each pixel further comprises an address transistor, connected between a power supply line and the gate of the drive transistor (see for example Fig. 6 item 9).

As to **claim 5**, in addition to the rejection of claim 4 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments further disclose means for disabling the driving of current by the drive transistor through the display element (see for example Fig. 5 noting that there is an "ILLUMINATING PERIOD" during which current driving of current through the display element is enabled and that during the rest of the driving period the driving of current by the drive transistor is disabled).

As to **claim 6**, in addition to the rejection of claim 5 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments disclose the claimed invention except for an isolating transistor in series with the drive transistor and the display element. It would have been obvious to one having ordinary skill in the art at the time the invention was made to add an additional transistor in series with the drive transistor of *Akimoto*, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co , 193 USPQ

8. In this case the two transistors would be driven on and off at the same time for example in order to reduce off state leakage current.

As to **claim 7**, in addition to the rejection of claim 4 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments further disclose disabling means comprising a switch for switching the voltage on one terminal of the display elements of the array of pixels (see for example Fig. 13 item 89). To further prosecution examiner also notes that an power switch for the device would also read on the claim limitation as written.

As to **claim 9**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments further disclose that the device is operable to provide pulse width modulation (see for example 3:34-4:27; note that).

Akimoto third and sixth embodiments do not explicitly disclose the device is operable in at least two sequential phases, one phase providing coarse resolution pulse width modulation and the other, shorter phase, providing fine resolution pulse width modulation. However, since Akimoto does not confine the device to a single speed of operation it is reasonable to assume that it may be operated at two or more speeds, i.e. one faster and thus having shorter pulses or finer resolution. Since it is operable at two speeds it is operable in at least two sequential phases at the two different speeds. This could be accomplished for

example by swapping oscillators or programming a different oscillation frequency.

Claim 10 claims the method implicit in the apparatus of claim 1 with the additional limitation that for a first set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned on, and for a second set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned off, the first and second sets being determined by the stored pixel drive level and is rejected on the same grounds and arguments as claim 1 with the additional argument that Akimoto third embodiment teaches the additional limitation (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter is on for period corresponding to a first set of steps indicated as being part of the "COLUMN ILLUMINATING PERIOD" and off for the rest or second set of steps).

The limitation of **claim 11** that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor was covered by the rejection of claim 10 since this was a limitation included in claim 1.

As to **claim 12**, in addition to the rejection of claim 11 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, claims the method implicit in the apparatus of claim 2 and is rejected on the same grounds and arguments.

As to **claim 13**, in addition to the rejection of claim 10 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, claims the method implicit in the apparatus of claim 3 and is rejected on the same grounds and arguments.

As to **claim 14**, in addition to the rejection of claim 10 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* further discloses that the act of storing a pixel drive level on the storage capacitor comprises turning on an address transistor (see for example Fig. 13 transistor 81) connected between a power supply line (see for example Fig. 13 item 87) and the gate of the drive transistor and charging the storage capacitor using the address transistor (see for example 12:51-55).

As to **claim 16**, in addition to the rejection of claim 10 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, claims the method implicit in the apparatus of claim 9 and is rejected on the same grounds and arguments.

As to **claim 17**, in addition to the rejection of claim 16 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* sixth and third

embodiments further disclose that the stepped voltage waveform to the input of the pixel has the same voltage levels in the two phases, and the shorter phase has shorter step transitions (since the sequential use of Akimoto from claim 16 changed only the speed one can reasonably assume that the voltage steps would remain the same).

4. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,876,345 to *Akimoto et al.* ("*Akimoto*") in view of "PIXEL-DRIVING METHODS FOR LARGE-SIZED POLY-SI AM-OLED DISPLAYS" by A. YUMOTO et al. ("*Yumoto*").

As to **claim 15**, *Akimoto* fifth embodiment discloses an active matrix electroluminescent display device comprising an array of display pixels (see for example column 5 lines 5-10 and column 1 lines 36-42), each pixel comprising: an electroluminescent display element (see for example Fig. 12 item 64 and column 11 line 38) and ; a drive transistor (see for example Fig. 12 TFT 70 and column 11 line 50) for driving a current through the display element, a drive voltage being provided to the gate of the drive transistor (see for example Fig. 3 and column 5 lines 40-42, which generally teaches to Vin to Vout relationship); and a storage capacitor (see for example Fig. 12 item 62 and column 11 lines 41-43) for storing a drive level (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55) and connected between an input to the pixel and the gate

of the drive transistor (see for example Fig. 12, which shows capacitor 62 so connected), the method comprising:

storing a drive level on the storage capacitor (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55);

providing a linear voltage waveform to the input of the pixel (see for example Fig. 14 "PIXEL DRIVING VOLTAGE" associated with "DRIVING SIGNAL LINE" and column 12 lines 55-60), the voltage waveform being voltage-shifted by the storage capacitor before application to the gate of the drive transistor (see for example Fig. 13 and column 12 lines 51-60, which describe the storage of a signal voltage on the capacitor followed by the application of a triangular waveform to the capacitor through line 96; this results in the triangular waveform being voltage-shifted by the amount of the stored signal voltage before being applied to the gate of the drive transistor), such that for a first set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned on, and for a second set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned off, the first and second sets being determined by the stored drive level (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter is on for period corresponding to a first set of steps indicated as being part of the "COLUMN ILLUMINATING PERIOD" and off for the rest or second set of steps);

Akimoto fifth embodiment does not expressly disclose that the voltage waveform is stepped.

Akimoto third embodiment discloses that the voltage waveform is stepped and that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor so that the linear operating region of the drive transistor is avoided (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter and thus the drive transistor, i.e. item 31 or 32 of Fig. 6, is off at one step and on at another, and further that setting the writing signal at a medium level ensures that the switch point, i.e. linear operating region, is crossed in the transition from one step to another; since this is indicated as a stepped transition the linear operating region is "avoided", that is the transition through this region is rapid).

Akimoto fifth embodiment and *Akimoto* third embodiment are analogous art because they are from the same field of endeavor, which is image displays capable of multilevel display, and seek to solve the same problem, which is to reduce the variation in PWM circuits caused by differences between TFT circuitry.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the stepped waveform of *Akimoto* third embodiment to the circuit of *Akimoto* fifth embodiment. The suggestion/motivation would have been to provide advantages such as to prevent changes caused by noise (see for example column 10 lines 11-14).

Akimoto third embodiment and *Akimoto* fifth embodiment do not expressly disclose disabling the driving of the current by the drive transistor through the display element during the storing of a pixel drive level on the storage capacitor.

Yumoto discloses a number of pixel driving circuits for OLED displays with at least two (Fig. 2 and 3) being circuits that store a voltage level on a capacitor and include a transistor (T4) that shuts of current flow through the drive transistor while the voltage level is stored. While, not specifically discussed, it is reasonably suggested to one of ordinary skill in the art at the time of the invention that at least one of the functions of this transistor is to prevent the OLED from illuminating during the storing of the voltage level.

Akimoto third embodiment and *Akimoto* fifth embodiment and *Yumoto* are analogous art because they are from the same field of endeavor, which is OLED displays.

Thus the prior art contains a base device, *Akimoto* third embodiment and *Akimoto* fifth embodiment, upon which the claimed invention can be seen as an improvement. This because *Akimoto* third embodiment and *Akimoto* fifth embodiment would allow a small but not necessarily zero current flow through the OLED from the drive transistor during storage of a voltage on the storage capacitor. We see that the prior art contained comparable devices, the pixel circuits of *Yumoto*, that have been improved in the same way as the claimed invention. One of ordinary skill in the art at the time of the invention could have applied the known improvement to the device of *Akimoto* third embodiment and

Akimoto fifth embodiment and the results would have been predictable to one of ordinary skill in the art, that is the current flow through the OLED during voltage level storage would be substantially eliminated.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide for disabling the driving of the current by the drive transistor through the display element during the storing of a pixel drive level on the storage capacitor as a modification of the device after *Akimoto* third embodiment and *Akimoto* fifth embodiment.

Allowable Subject Matter

5. **Claim 8** allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: Examiner is interpreting the phrase "means for disabling the driving of the current by the drive transistor through the display element" in claim 8 under 112 6th paragraph, which limits the "means for" to switch 34 and equivalents. The specification at [0050] 9:10-17 describes an alternative, that of a switch in the power or ground line that affects all pixels, but this alternative is excluded by the requirement in claim 8 that the means be part of each pixel, i.e. "each pixel comprising". If not interpreted this way, the other elements listed as comprising each pixel could then also be said not to be duplicated inside each pixel but just somewhere between power generation and the OLED element. The art of record does not disclose a first mode in which a pixel voltage is applied to the input to the pixel, the address transistor is turned on, the disabling

means is turned on to turn off the display element and the storage capacitor is charged to a level derived from the drive voltage in addition to the other limitations of claim 8. Note that Akimoto in Fig. 17 and 18 shows as prior art a circuit described at Akimoto 1:43-2:39 that includes means for disabling the driving of current (Fig. 17 transistor 223) by the drive transistor through the display element during the storing of a pixel drive level voltage on the storage capacitor, but this prior art circuit is not taught as operating in a PWM manner from a stepped waveform with steps larger than the linear region of the drive transistors and the function of the circuit of Akimoto Fig. 13 would be destroyed by the addition of an isolation transistor as shown in Akimoto Fig. 17 because the charging path for the capacitor during the writing phase would be lost.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629